ISBN 978-93-84468-20-0
Proceedings of 2015 International Conference on Future Computational Technologies (ICFCT'2015)
Singapore, March 29-30, 2015

Enhancement of SAR Algorithm for Analog to Digital Converter

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***Abstract*:** Nowadays, the development of the IC technology resulted in a growth of digital systems. Thus, Analog to Digital converters have become important. The important criteria of an ADC are resolution, speed and power. Among them, speed plays an important role to be enabling faster and more reliable for data processing. This paper describes a successive approximation ADC that uses a charge-redistribution digital- to-analog converter (DAC) designed to achieve a good accuracy and high speed. However, conventional Successive Approximation Register (SAR) ADC can get the final conversion result through a total of "n" time comparison to convert "n" bits digital code from an analog. This makes SAR ADCs that is not affected for high speed applications. To overcome this problem, the new algorithm of SAR ADC which can reduce the number of conversion step is proposed. This algorithm enhances the speed of SAR ADC system that to be apply in high speed application.

Keywords: *SAR, speed, ADC, accuracy, resolution.*

1. Introduction

In many mixed-signal systems, Analog-to-Digital Converters (ADCs) are required for interfacing analog signals to digital. The requirement is usually to integrate these ADC's with microcontrollers or digital signals processors .The integrated ADC's are required to operate in the same range of supply voltage. The important thing in design an ADC is operating such a low voltage supply, with high speed [1]. The ADC is designed for low-power, medium-quality applications. Fig.1 shows that different types of ADC. Among the data converter architectures, the flash is a first generic option; it uses (2^n-1) comparators, where "n" is the number of bit. The architecture will get too power hungry because of high comparator number even for low resolution. Also the pipeline architecture is not a suitable approach for ultra low-power applications. Each stage uses an active gain element whose power equals the one of many comparators. Therefore, it becomes competitive for high resolution. On the other hand sigma-delta and the time interleaved have similar limit because of their speed or multiple paths to increase resolution or throughput, they use active power hungry elements [2].However, if the speed and resolution are medium the most suitable algorithm is the SAR that uses a successive approximation register (SAR) to control a DAC in a feedback loop with a single comparator.

However, modern portable and wireless applications are diving analog-to-digital converters (ADCs) design towards higher resolution and data rates with dramatically low power in scaled CMOS technology. Pipelined ADCs have been facing significant challenges with technology scaling since accurate residue amplification in each pipelined stage based on op-amplifier's property is required. Successive Approximation Register SAR ADC can benefits from the scaled CMOS because it does not need amplifier and most of the part switched capacitors and comparator, are digitally operation. Charge redistribution based capacitor DAC (CDAC) is widely used for SAR ADCs because of its superior response to resistor DAC (RDAC). SAR ADC has become a main stream in

application for moderate speed and high resolution region due to the advantage of power and area efficiencies [3].

Conventional SAR ADCs are difficult to be applied in high-speed design; however the improvements of technologies and design methods have allowed the implementation of high-speed and low-power SAR ADCs. In this situation, the new SAR algorithm is developed to get higher speed of ADC by reducing steps in a converting process. In this paper, the proposed algorithm intends SAR ADC to get high speed and to easily be applied in high-speed application technology.

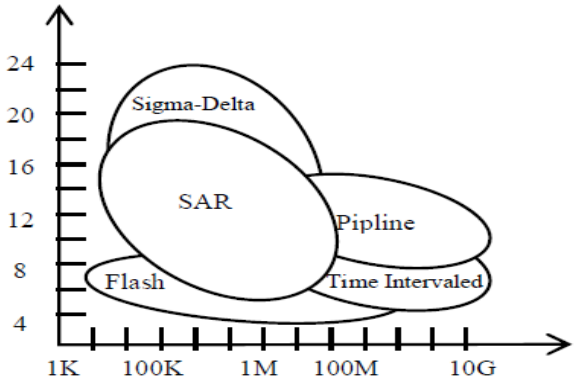

Fig.1 : Sampling rate versus Resolution of various ADC's types.

2. Conventional Successive Approximation Register (SAR) ADC

Successive approximation ADC is most generally and dominantly used method of analog to digital conversion in many of available IC's because of its high performance and low power consumption. As shown in Fig.2, it consists of a Sample/Hold (S/H) circuitry, a comparator, a DAC, and a successive approximation register. A sample/hold circuitry is used to perform sampling of the analog input and hold the sampled value while the binary search is being performed. A DAC is used to convert the digital value received from the SAR into the analog value by utilizing the reference voltage. The SAR is used to supply an approximate digital signal of input analog voltage to the DAC. The drawback of this approach is that it consumes high power and takes longer time due to separate S/H circuit [4].

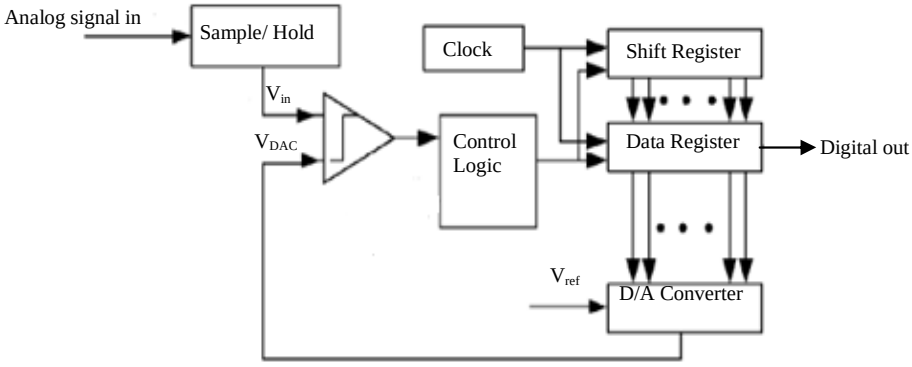

Fig .2: Block Diagram of Conventional SAR ADC Module.

2.1. Conventional Successive Approximation Algorithm

Successive approximation ADC uses binary search algorithm to perform the conversion from analog signal to digital signal. Here, it is presented the working principle of successive approximation ADC. The step by step process of this conversion algorithm using binary search is described below [5].

- Initially, DAC input set to midscale (MSB = 1)
    - if $V_{in} > V_{DAC}$, MSB remains 1
    - if $V_{in} < V_{DAC}$, MSB set to 0
- Then the next bit is set to 1 and the algorithm is repeated until LSB
- At the end of algorithm, ADC output is the DAC input

Thus for "n"-bit successive approximation ADC, "n"-comparison is performed by the internal circuitry of ADC before the digital equivalent of the analog input signal is obtained.

3. Proposed Successive Approximation Register (SAR) ADC

The architecture of an SAR ADC based on proposed algorithm is shown in Fig. 3, consisting of a series structure of a capacitive DAC, a comparator, successive e approximation (SA) control logic, two operational amplifiers and two comparators. A capacitive DAC is used to convert the digital value received from the SAR into the analog value by utilizing the reference voltage and input voltage. The DAC capacitor array is the basic structure of the SAR ADC and it serves both to sample the input signal and as a DAC for creating and subtracting the reference voltage. Thus, this system is no needs external Sample and Hold circuit. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. The proposed architecture is defined: $V_x=V_{DAC}-V_{in}$, $V_{out1}= 0.5$ LSB, $V_{out2}= V_x- 0.5$LSB.

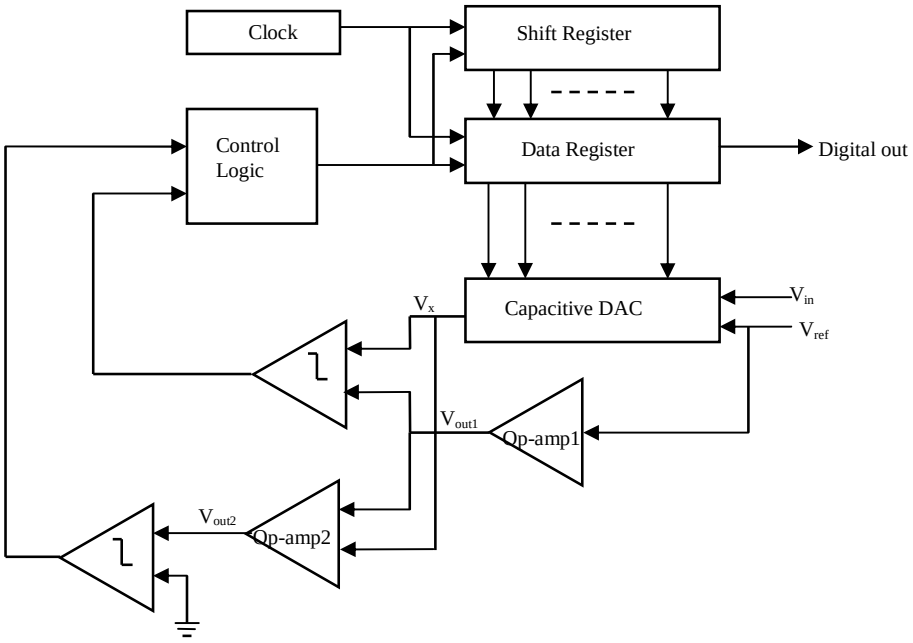

Fig .3: Block Diagram of Proposed SAR ADC Module.

3.1. Proposed Successive Approximation Algorithm

The proposed algorithm is based on conventional binary search algorithm for getting good speed of analog to digital converter to use in high speed application such as wireless sensor network. The speed of SAR ADC determines the time requiring by the DAC to settle within ½ LSB. Depending on this fact, the proposed algorithm is to turn out the result code before the cycle counter reaches the final value. The step by step process of the proposed conversion algorithm using binary search is described below:

- Initially, DAC input set to midscale (MSB = 1)
- if $V_{DAC}-V_{in} \leq 0.5$LSB, stop the process

- ADC output is the DAC input
    - if $V_{DAC} - V_{in}$ -0.5LSB < 0 , MSB remains 1
    - if $V_{DAC} - V_{in}$ -0.5LSB > 0, MSB set to 0
- Then the next bit is set to 1 and the algorithm is repeated until $V_{DAC} - V_{in} \leq 0.5LSB$

Therefore, "n"-bit successive approximation ADC, k< n-comparison is performed by the internal circuitry of ADC before the digital equivalent of the analog input signal is obtained. The main advantage of this proposed design is its minimization of time due to reduce the number of conversion steps and its low power consumption due to inherent sample-and-hold operation inside the capacitive DAC.

4. Flow Diagram of Conventional and Proposed SAR Algorithm

The design of SAR control logic based on SAR algorithm. The flow diagram of the conventional and proposed successive approximation algorithm is shown in Fig. 4 and Fig. 5. In the conventional SAR ADC, successive approximation register (SAR) control logic determines each bit successively. "n" bit SAR ADC takes "n" clock cycles to perform a conversion [6].

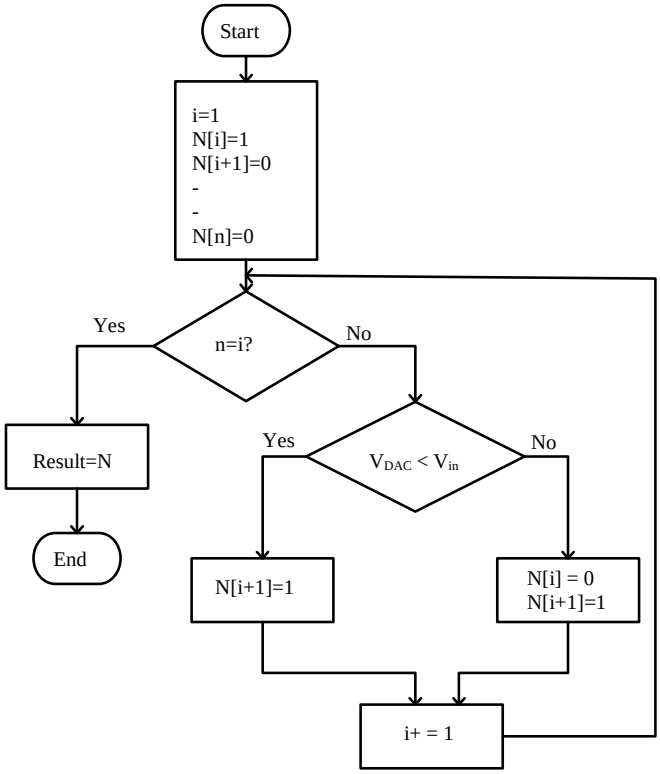

Fig. 4: Flow Diagram of Conventional SAR Algorithm.

Firstly, a "N" register array is defined. It has N[i]…N[n], where "n" is the number of bits and "i" is number of count of the register. And then, set i=1, therefore N[i]=1 ,N[i+1]=0, N[i+2]=0,…,N[n]=0. This means that Most Significant Bit (MSB) set to 1 and other bits set to 0.

Secondly, we can test n=i?, it means "Does the current condition reach to the Least Significant Bit (LSB)?". If "n" is equal "i", the result is N array and sends out the result code. And then, the process is finished.

If not, thirdly, we can test V_{DAC} and V_{in}, where, V_{DAC} is the voltage changes from digital to analog and V_{in} is input voltage of the device. In this condition, if $V_{DAC} < V_{in}$, the next bit set to "1" and the current bit reset to "1". It is N[i]=1 and N[i+1]=1. Otherwise, if $V_{DAC} > V_{in}$, the next bit set to "1" and the current bit change to "0". It is N[i]=0 and N[i+1]=1. And then, the counter increases one. In this way, the process continues until at the end of

the least significant bit. Finally, when the test condition reaches the least significant bit, the process is done and sent out the result code of digital value. It means that for "n" digit private it is necessary to execute "n" steps.

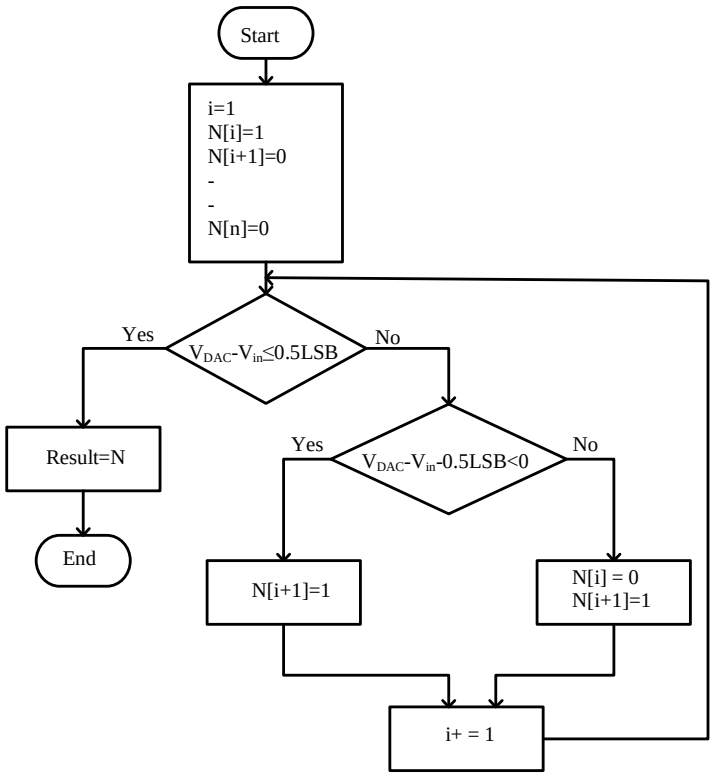

Fig. 5: Flow Diagram of Proposed SAR Algorithm.

According to the proposed algorithm, in the second stage, tests the operation of V_{DAC}-V_{in} and 0.5 LSB value, where, V_{DAC} is the voltage changes from digital to analog and V_{in} is input voltage of the device. If V_{DAC}-$V_{in} \leq$ 0.5 LSB, the process stops and sends out the current result code in the N register array. This result is valid to desire digital code. It means that the proposed system can reduce the number of conversion steps less than the number of bits. If not, the process goes to the next step.

In the next stage, we can test V_{DAC}-V_{in}-0.5LSB and 0. In this condition, if V_{DAC}-V_{in}-0.5LSB < 0, the next bit set to "1" and the current bit reset to "1". It is N[i] =1 and N[i+1] =1. Otherwise, if V_{DAC}-V_{in}-0.5LSB > 0, the next bit set to "1" and the current bit reset to "0". It is N[i] = 0 and N [i+1] =1. And then, the counter increases one. In this way, the process is continued until at V_{DAC}-$V_{in} \leq$ 0.5 LSB. Finally, when the test condition is satisfied, the process is done and sent out the valid digital value.

The number of conversion steps for proposed system SAR ADC can be reduced less than the number of bits (k < n) where, k is the performance conversion step of proposed ADC and "n" is the number of bit. The number of conversion cycle is difference such as more or less upon the various values of input voltage and reference voltage.

5. Methods and Results

In this section, reduction of number of cycles and reduction of percentage of average time methods are presented. These methods are based on the proposed algorithm. According to these methods, the proposed ADC decreases the conversion steps when comparing the conventional system. These methods are described depending on the number of bit 'n'. These methods are shown as follows:

$$\text{Reduction of the number of cycles} = 2^n - (n+1) \quad (1)$$

$$\text{Reduction of percentage of average time} = \left[\frac{\left[2^n - (n+1)\right]}{2^n \times n}\right] \times 100\% \quad (2)$$

According to these methods, Fig. 6 and Fig. 7 show reducing for conversion time and conversion step of the proposed algorithm with the various numbers of bits. The result of percentage of average time reducing is shown in Table 1and Table 2. The 5-bits operation is reduced about 16.25%, the 11-bits operation is reduced about 9.04% and the 17-bits operation is reduced about 5.88% based on these methods.

TABLE I: Percentage of Time Reducing for Odd Bits

No: of Bit	No: of cycle Reducing	% of Time Reducing
5	26	16.25
7	120	13.39
9	502	10.89
11	2036	9.04
13	8178	7.68
15	32752	6.66
17	131054	5.88

TABLE II: Percentage of Time Reducing for Even Bits

No: of Bit	No: of cycle Reducing	% of Time Reducing
4	11	17.19
6	57	14.84
8	247	12.06
10	1013	9.89
12	4083	8.31
16	65519	6.23
18	262125	5.56

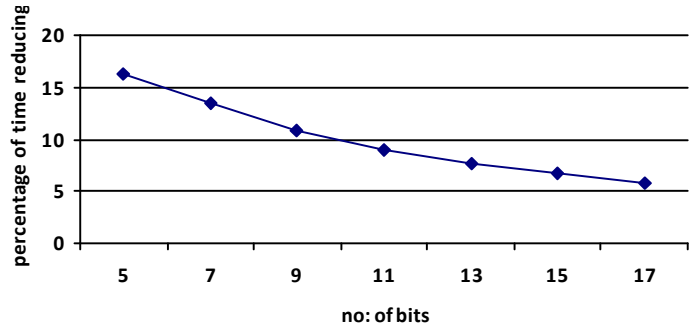

Fig .6: Conversion Time Reducing.

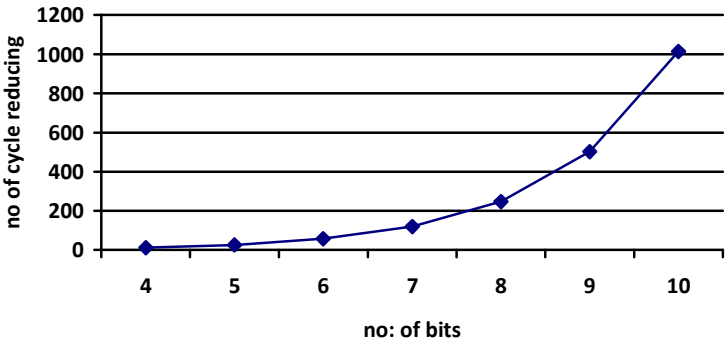

Fig .7: Conversion Step Reducing.

6. Conclusion

Based on the proposed SAR algorithm, the new design of successive approximation register (SAR) ADC has been improved. Here, the main idea of this system is to enhance the speed SAR ADC by using the proposed SAR algorithm. According to the conversion time reducing graph, the proposed ADC decreases the conversion steps from 5% to 16%. In addition, the capacitive DAC with inherent Sample and Hold consumes less power and time and it induce less mismatch errors compared to the resistive based DAC. Therefore, the conversion time of proposed SAR ADC can be reduced more than conventional system.

7. Acknowledgements

The author would like to thank to all people for their invaluable advices, encouragements and overall supporting in writing of this paper.

8. References

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